## REMARKS

In the Office Action, the Examiner indicated that Claims 1-5 and 7-9 are pending in the application and the Examiner rejected all pending claims.

### Claim Rejections, 35 U.S.C. § 102

On page 3 of the Office Action, the Examiner rejected Claims 1, 3, 4, and 7-9 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,396,131 to Miki et al. ("Miki").

### The Cited Prior Art Does Not Anticipate the Claimed Invention

The MPEP and case law provide the following definition of anticipation for the purposes of 35 U.S.C. §102:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 citing *Verdegaal Bros. v. Union Oil Company of California*, 814 F.2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)

### The Examiner Has Not Established a *Prima Facie* Case of Anticipation

The present claimed invention teaches a switch circuit wherein each biasing transistor of a first circuit portion is coupled at its base to a base of a corresponding biasing transistor of a second circuit portion. Specifically, Claim 1 recites:

> A switch circuit comprising:
> a first circuit portion corresponding to a first input port;
> a second circuit portion corresponding to a second input port; and
> an output port,

> wherein each of the first and second circuit portions include at least one first transistor providing a portion of an isolation channel, at least one second transistor providing a portion of a transmit channel, and at least two third transistors for providing a control bias for selecting either the transmit channel or the isolation channel; and
>
> wherein each third transistor of the first circuit portion is coupled at its base to a base of a corresponding third transistor of the second circuit portion, and to a control voltage source.

As detailed in the specification of the present invention, coupling the third transistor of the first circuit portion to the third transistor of the second circuit portion allows a control voltage source to control a voltage applied to a bias transistor from each circuit portion, thereby permitting a signal transmitted from the first input port to appear at the output port while simultaneously isolating a signal transmitted from the second input port, and vice versa. This simultaneous transmitting/isolation provides the switching function of the switch circuit and defines the present invention as novel over the prior art of record.

Miki, to the contrary, is directed to a high speed analog-digital (A/D) converter. The high speed A/D converter of Miki includes a differential amplifier circuit for comparing an applied analog input voltage and an applied reference voltage. Figure 10 is relied upon by the Examiner in his rejections of Claims 1, 3, 4, and 7-9, and is representative of the system taught by Miki. In Figure 10, differential amplifier circuit 400e fails to disclose wherein each third transistor of the first circuit portion is coupled at its base to a base of a corresponding third transistor of the second circuit portion, and to a control voltage source as claimed which provides for the switching functionality of the present invention. Specifically, Figure 10 lacks a biasing transistor of a first circuit portion being coupled at its base to a base of a corresponding third transistor of the second portion.

The Examiner asserts biasing transistors 305 and 306 of Figure 10 are the third transistors of a first circuit portion and are connected via lines $I_{10}$ and $I_{20}$ to corresponding third transistors in a second circuit portion. Applicant respectfully disagrees with the Examiner's interpretation of Figure 10 of Miki. The biasing transistors 305 and 306 connect at their bases to each other and to a voltage source. No other connections are made at the bases of the transistors. Certainly no connection to any component in the second circuit portion is made at the base of transistors 305 and 306. Rather, any connections between transistors 305 and 306 are made via the collectors of each transistor and additional circuit components (such as transistors 301, 302, 303, 304, 301', 302', 303' and 304'). Even these connections between the third transistors would be made at the collectors of the transistors, not the bases. The collectors and the bases of transistors function in very different and distinct manners. Bases are used as control inputs for transistors, determining whether charges accumulated at the collector are passed through to the emitter. Collectors function as their name implies, by collecting a charge and, depending on the state of the base, passing the charge to the emitter. Connecting the collectors of two transistors is well known in the art and is not considered by the inventors to be novel. What is novel is connecting the bases of the third transistors to provide a transmitting/isolation switching circuit, as is specifically claimed by the present invention.

This limitation is specifically claimed in each independent claim (Claims 1 and 9). Accordingly, Claims 1, 9, and all claims depending therefrom, patentably define over Miki and are in condition for allowance. Applicants respectfully request that the Examiner's rejections of Claims 1, 3, 4, and 7-9 under 35 U.S.C. §102 be withdrawn.

**Claim Rejections, 35 U.S.C. § 103**

On page 4 of the Office Action, the Examiner rejected Claim 2 under 35 U.S.C. §103(a) as being obvious over Miki in view of U.S. Patent No. 3,798,376 to Limberg. Additionally, on page 5 of the Office Action, the Examiner rejected Claim 5 under 35 U.S.C. §103(a) as being obvious over Miki in view of U.S. Patent No. 4,460,873 to Hester.

**The Examiner Has Not Established a *Prima Facie* Case of Obviousness**

As set forth in the MPEP:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
> MPEP 2143

As discussed above, Miki fails to teach claimed limitations of the present invention, specifically wherein each third transistor of the first circuit portion is coupled at its base to a base of a corresponding third transistor of the second circuit portion, and to a control voltage source. Limberg teaches a decoder circuit for stereophonic FM broadcast receivers adapted for construction by integrated circuit techniques. Limberg is not concerned with providing a transmitting/isolation circuit and does not teach or reasonably suggest each third transistor of the first circuit portion being coupled at its base to a base of a corresponding third transistor of the second circuit portion, and to a control voltage source. Similarly, Hester teaches a feedback loop

for adjusting the voltage output of a differential amplifier. Hester is not concerned with providing a transmitting/isolation circuit and does not teach or reasonably suggest each third transistor of the first circuit portion being coupled at its base to a base of a corresponding third transistor of the second circuit portion, and to a control voltage source. Without such a teaching or suggestion, the present invention is non-obvious over the prior art of record, specifically Miki, Limberg and Hester, whether considered alone or in any combination.

Accordingly, Applicant respectfully submits that Claims 2 and 5 are patentable over Miki in view of Limberg or Miki in view of Hester under 35 U.S.C. §103. Applicant respectfully requests the Examiner to reconsider and withdraw the rejections of Claims 2 and 5 under 35 U.S.C. §103.

**Conclusion**

The present invention is not taught or suggested by the prior art. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejection of the claims. An early Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 19-5425.

Respectfully submitted,

July 20, 2007
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